AMENDMENTS TO THE SPECIFICATION

Please add a new paragraph on page 6 after line 22 as follows:

Figure 22 represents an exemplary structure of one embodiment of the communication device.

Please amend the paragraph on page 7, starting on line 19 as follows:

The transmitter 1 contains a plurality of QPN channels 3 as shown in Figure 2. These channels are, for example, combined in two sets of four QPN channels (set A and set B) and a set C with only one QPN channel, as shown in Figure 1. Each set has a separate block for generating a PN-code 5 and a separate synchronization hardware 7, which defines a start of symbol transmission. A processor 10 is in data communication with the transmitter 1 and provides operational parameters for the transmitter. The transmitter 1 and processor 10 are also shown as part of a communication device/integrated circuit 20 shown in Figure 22.

Please amend the paragraph starting on page 7, line 26 through page 8, line 3 as follows:

An output of the synchronization hardware 7 goes to the QPN channels of a set and defines a common symbol start moment for all QPN channels in a set. This signal is generated as a selection of one out of a plurality of incoming signals with a programmable offset. The incoming sync channels may, for example, be generated by: another chip, TX timers, receiver pulse, signal acquisition ~~hardware~~ component 9 output, or the like. In certain embodiments, the signal acquisition ~~unit~~ component 9 connects to each synchronization hardware 7. The processor 10 is in data communication with the signal acquisition ~~unit~~ component 9. The signal acquisition component 9 and the synchronization hardware are also shown as part of the communication device 20 shown in Figure 22. In one embodiment, a counter at the chip rate may be used to generate the offset. This gives an offset resolution of one 'primary' chip. The range of the offset is [0:65535]. This is sufficient to give an offset of one frame for UMTS (40960 chips).

Please amend the paragraph starting on page 8, line 10 as follows:

Input binary symbols coming directly from an interface (symbI 13 and symbQ 14) are spread with PNbits PNbitI and PNbitQ. Each symbol has an activity bit (actI and actQ). When this is 0 the functional spreader output will be 0 instead of +1 or -1. This activity bit is used for burst transmission and for BPSK instead of QPSK/QPN transmission. Signals symbI and actI are signals at a symbol rate fsIxx. Signals symbQ and actQ are signals at a symbol rate fsQxx. The symbol rate fsIxx may differ from the symbol rate fsQxx. The spreading factor is set by a sfI input 15 and a sfQ input 16. The sfI input 15 and the sfQ input 16 are two of the first parameters 22 (Figure 22) that are used to configure the spreader 11, which is a part of the transmitter 1 (Figures 1 and 22). Other first parameters 22 that are used to configure the spreader 11 are indicated by the dashed boxes as shown in Figure 2. The first parameters 22 for the transmitter 1 are received from the processor 10 and are stored in memory 23 comprising a first RAM and/or first registers. The spreaders may be (re)started via a sync signal 17 obtained from the acquisition unit 9 via the synchronization hardware 7. A rate fcp is defined as: fcp=fsIxx * sfI = fsQxx * sfQ.

Please amend the paragraph starting on page 14, line 1 as follows:

The global receiver structure 43 is shown in Figure 8. The processor 10 is in data communication with the receiver 43 and provides operational parameters for the receiver. The receiver 43 and processor 10 are also shown as part of the communication device 20 shown in Figure 22. All functional blocks are discussed in more detail in the next paragraphs.

Please amend the paragraph starting on page 15, line 6 as follows:

The noise estimator 63 (Figure 10), which is also known as a reference demodulator, provides a filtered complex noise correlation value which may be read by the microcontroller subsystem such as processor 10. This value could be used for setting thresholds in the acquisition hardware. The noise correlator 65 is just the accumulation of NC_length absolute values 64 of the complex input. In this way, an RSSI estimation is obtained. The filter is a hardware low-pass filter. By setting the bypass to 1, the low-pass filter may be bypassed. The NC_length 64 and bypass are two of the second parameters 22' (Figure 22) that are used to

configure the noise estimator/reference demodulator 63, which is a part of the receiver 43 (Figures 8 and 22). Other second parameters 22' that are used to configure the level control 53 in the receiver 43 are indicated by the dashed boxes as shown in Figure 9. The second parameters 22' for the receiver 43 are received from the processor 10 and are stored in memory 23' comprising a second RAM and/or second registers.

Please amend the paragraph starting on page 22, line 5 as follows:

The incoming chips are descrambled with Psb. This code and its phase are common for all fingers. The phase has to be set during an acquisition process initializing the Rake via the signal acquisition ~~unit~~ component 9. The descrambler 117 has the same functionality as the other descramblers.

Please amend the paragraph starting on page 22, line 10 as follows:

The complex signal coming from the descrambler 117 at the chip rate is despread with the pilot Pncode (Pcb), only one despreader, so the pilot must be a QPSK or BPSK signal. The pilot PNcode has a PNlength of Psf, wherein 4<=Psf<-256, and k*Psf=2560 with k being a positive integer. The despreader 119 works continuously and is synchronized, via the signal acquisition ~~unit~~ component 9, to the slot edge at chip rate. This means that a new symbol starts at the start of the slot (slot-edge=1).